Abstract

Multilevel inverters have inherently superior harmonic performance compared to the conventional 2-level inverter and hence they can be operated at a lower switching frequency. Different topologies have been proposed in literature for multilevel inverters and this thesis investigates multilevel topologies for the induction motor in the open-end winding configuration. The open-end winding configuration is realised by opening the neutral point of the star connected stator of the conventional induction motor. Multilevel inverter structures can be realised by feeding the open-end winding induction motor from both sides. The multilevel inverter topologies proposed in the thesis uses this dual inverter fed open-end winding configuration for the induction motor. A 5-level inverter scheme and a 9-level inverter scheme are proposed in this thesis and these topologies are realised using the conventional 2-level inverters. The modulation schemes adopted for multilevel inverters can be viewed as the extended forms of those employed for the conventional 2-level inverters. Both the Sinusoidal Pulse Width Modulation (SPWM) and the Space Vector based Pulse Width Modulation (SVPWM) are employed for the multilevel topologies presented in this thesis. A space phasor based Current Hysteresis Controller is also proposed in this thesis. This thesis also investigates the suitability of the multilevel inverter structure using open-end winding configuration, for eliminating the common mode voltage in the inverter-drive system.

A topology for voltage space phasor generation equivalent to a 5-level inverter for an open-end winding induction motor is presented in Chapter 2. The open-end winding induction motor is fed from both ends by two 3-level inverters. The 3-level inverters are realised by cascading two 2-level inverters. The individual 2-level inverters use separate DC link of $\frac{V_{dc}}{5}$ each where V_{dc} is the full DC link voltage of the conventional 2-level inverter. This inverter scheme does not experience neutral point fluctuations. Of the two 3-level inverters only one inverter will be switching at any instant in the lower speed ranges. In the

multi level carrier based SPWM used for the proposed drive, a progressive discrete DC bias depending upon the speed range is given to the reference wave to reduce the inverter switchings. With this modulation scheme depending upon the speed, the inverter operates initially in the 2-level mode and then moves to the 3-level, 4-level and finally to the 5-level mode of operation. the drive is implemented and tested with a 1.5kW open-end winding induction motor and the experimental results are presented.

In Chapter 3, a topology for high resolution voltage space generation for an open-end winding induction motor drive is presented. The open-end winding induction motor is fed from both ends by two 3-level inverters with asymmetrical DC links. It is shown that this results in voltage space phasor levels equivalent to a conventional 9-level inverter. One of the 3-level inverters is realised by cascading two 2-level inverters with DC link voltage of $\frac{3}{8}V_{dc}$ each and the other 3-level inverter is realised by cascading two 2-level inverters with DC link voltage of $\frac{1}{8}V_{dc}$ each. Compared to the H-bridge topology, the proposed scheme uses a lower number of power supplies. In the multi carrier Sinusoidal Pulse Width Modulation used for the proposed drive, a progressive discrete DC bias depending upon the speed range is given to the reference wave so that the drive can operate in the i-level modes ($i = 2, 3,..9$) depending on the speed range. This modulation scheme ensures that the inverter with the larger DC-link voltage is switching less frequently, compared to the inverter with the smaller DC-link voltage. The drive is implemented and tested with a 1.5kW open-end winding induction motor drive and the experimental results are presented.

In Chapter 4, a space vector based PWM method using only the instantaneous amplitudes of the reference phase voltage amplitudes is proposed for the 3-level inverter. The voltage space phasors of a 3-level inverter are situated in 19 locations forming 24 triangular sectors. The instantaneous reference voltage space phasor is generated by switching between the three adjacent vectors forming the sector in which the tip of the reference vector lies. The proposed scheme ensures that the middle vectors are always centered within an inverter

switching time period. The proposed SVPWM method does not require the sector identification and look up tables to select the appropriate vectors. The inverter leg switching times are directly obtained from the instantaneous reference phase voltage amplitudes and the inverter switching vectors are automatically generated. The inverter leg switching times and the appropriate vectors are obtained using an algorithm, which does not involve computations like square root or coordinate transformations. The proposed method is implemented on a 1.5kW induction motor drive and the experiment results are presented.

A space phasor based current hysteresis controller for a three phase voltage source inverter is proposed in Chapter 5. The conventional hysteresis controller uses independent comparators for the three phases and the output of each of the comparator controls the top switch of the respective inverter leg so that in each phase, the machine current is kept within a hysteresis band. The space phasor based current hysteresis controller uses appropriate inverter voltage vectors so that the instantaneous current error space phasor is kept within a boundary. In the space phasor based current hysteresis controller proposed in this thesis, the instantaneous current errors are determined along three axes, which are orthogonal to the A, B, C phases, and the current error space phasor is held within a hexagonal boundary. The proposed controller does not require any computation of machine voltage vector and uses only those inverter voltage vectors, which are adjacent to the machine voltage vector for the entire range of operation. The region detection logic employed in the proposed controller ensures that, the vector (among the three adjacent vectors), which has the largest deviation in the opposite direction, is selected, for all the regions of the hexagonal boundary. A simple, self adapting logic is used to effect sector changes and smooth transition to six step mode of operation is achieved. The proposed controller is implemented for a 5HP induction motor drive and the results are presented.

In Chapter 6, a dual inverter scheme with open-end winding induction motor configuration is proposed for eliminating the common mode voltage in the inverter-drive system. PWM Inverters are known to generate common mode voltages which cause motor

bearing currents in the induction motor drives. They also result in leakage currents which act as sources of conducted electromagnetic interference in the drive system. The common mode voltage generated by a conventional 3-level inverter can be eliminated by switching only the voltage space vectors which do not produce the common mode voltage. A PWM switching strategy to eliminate common mode voltage using the open-end winding configuration for the induction motor is proposed. The switching strategy presented in this chapter, does not generate any alternating common mode voltages in the drive system and hence the electrostatic coupling of the common mode voltage, which results in the bearing currents and the leakage currents, is avoided. The proposed scheme is devoid of neutral point voltage fluctuations and does not require neutral point clamping diodes, when compared to the common mode elimination scheme based on the conventional 3-level inverter topology. Also, the proposed scheme uses a single DC-link with half the voltage compared to the common mode voltage elimination scheme based on the conventional 3-level inverter.

All the schemes presented in this thesis have been simulated with SIMULINK/MATLAB tools before verifying experimentally. All the schemes except the current hysteresis controller have been implemented digitally on the TMS320F240 platform while the current hysteresis controller has been implemented on the TMS320F2407 processor. The experimental results are in agreement with the simulation results.

The multilevel inverter topologies and modulation strategies presented in this thesis are particularly suitable for high power applications such as traction and electric drives. All the proposed scheme have been experimentally verified using low power laboratory prototypes. But the proposed control and PWM techniques are general in nature and can be easily applied to inverter fed induction motor drives of high power applications.